94 GHz POWER AMPLIFIER USING PHEMT TECHNOLOGY

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ABSTRACT

A millimeter wave power amplifier has been developed using power MMICs based on 0.10 micron T-gate pseudomorphic HEMT technology. It uses four MMIC chips in parallel with a low loss 4-way power combiner with two cascaded driver amplifier stages. The amplifier module demonstrated 100 mW output power with more than 32 dB linear gain at 94 GHz. These results are attributed to the excellent device and combiner performance.

INTRODUCTION

94 GHz is the frequency of interest for missile seeker and radar applications. In the past, the transmitter components in these frequencies were usually based on IMPATTs and suffered from size contraints. Recent technical advances using super-lattice HEMT structures have resulted in devices that exhibit high power and higher efficiencies in frequencies through 150 GHz. Using different levels of low-loss combiners it is possible to realize amplifiers with output powers greater than 350 mW at 94 GHz. This paper reports on a 100 mW output power amplifier module that uses 35 mW power chips as the building block for higher power SSAs. The basic components and details about the power modules and the combining methodology are described in this paper.

Device Technology

The devices used for the MMIC development are pseudomorphic 0.1 micron "T" gate HEMTs (InGaAs/GaAs).These HEMTs provide higher breakdown voltage and current density producing more power than the conventional (GaAlAs/ GaAs) HEMTs. These devices are fabricated using MBE material and E-beam lithography and offer high efficiencies and gain at millimeter wave frequencies.

MMIC Development

The MMIC development involves detailed device modeling and characterization. A large signal model was developed, and the input matching network was optimized for maximum gain, while the output was matched for maximum power. A photograph of the basic device is shown in Figure 1.

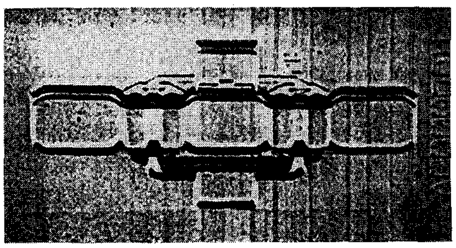

Figure 1. Photograph of pseudomorphic HEMT device.

The power chip as shown in Figure 2 is a three stage design that provides 8-10 dB gain with 15-16 dBm output power at 94 GHz. A plot of chip's input power versus the output power is shown in Figure 3. This chip is used as both as the driver amplifier and the output power amplifier chips. The pre-driver amplifier is also a three stage MMIC chip that uses two single ended stages to drive a balanced output stage. A photograph of this MMIC amplifier chip is shown in Figure 4. This chip has demonstrated 15-18 dB linear gain and 11 dBm output power as shown in Figure 5.

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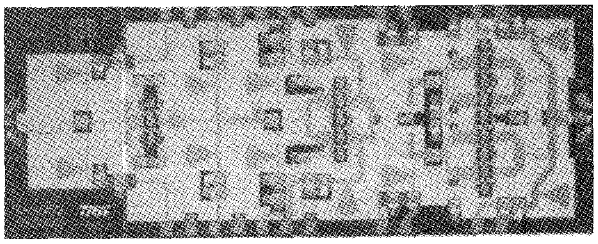

Figure 2. Photograph of MMIC power amplifier chip.

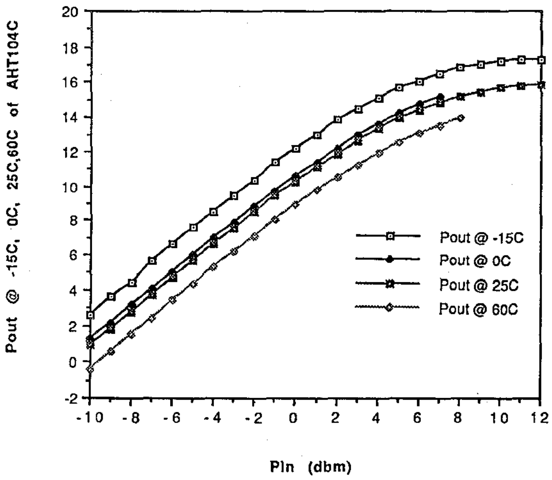

Figure 3. Plot of input power versus output power.

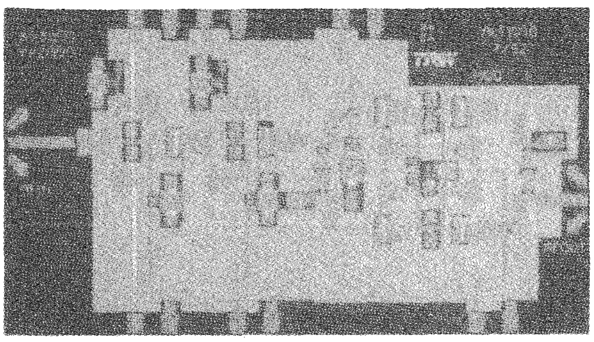

Figure 4. Photograph of MMIC pre-driver amplifier .

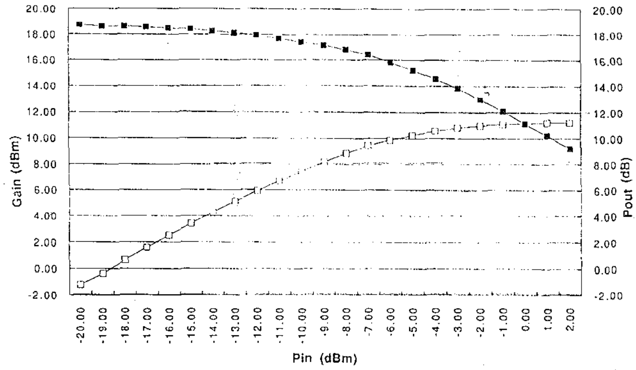

Figure 5. Plot of input versus output power for pre-driver amplifier.

Planar Combiner

Millimeter wave Wilkinson power combiners have been developed at 94 GHz. Several combiners including 2-, 3-, and 4-way have been demonstrated with low loss. These were fabricated on 0.005-inch thick fused silica substrate. Figure 6 shows the back-to-back realization of a 4-way planar combiner. The uncorrected transmission loss for two 4-way dividers placed back-to-back path is 3.9 dB, this number includes 1.4 dB for fixture loss. The loss for a single combiner is 1.25 dB, after correcting for the test fixture loss. Transmission loss data for the for the 4-way power divider is shown in Figure 7. Deposited thin-film resistors are used to give the combiner excellent port-to-port isolation and VSWR. The dividers have been laid out so that the phase from all four amplifiers are equal at the output port.

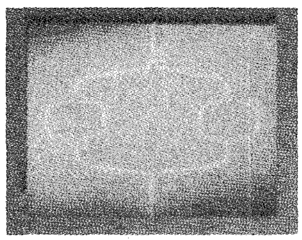

Figure 6. Photograph of Wilkinson 4-way power divider.

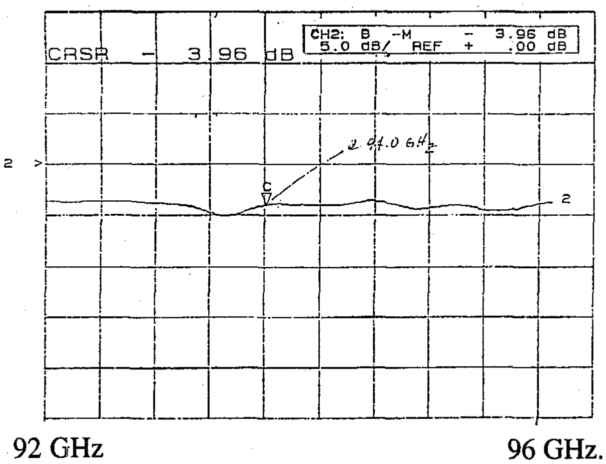

Figure 7. Performance of 4-Way Wilkinson power divider.

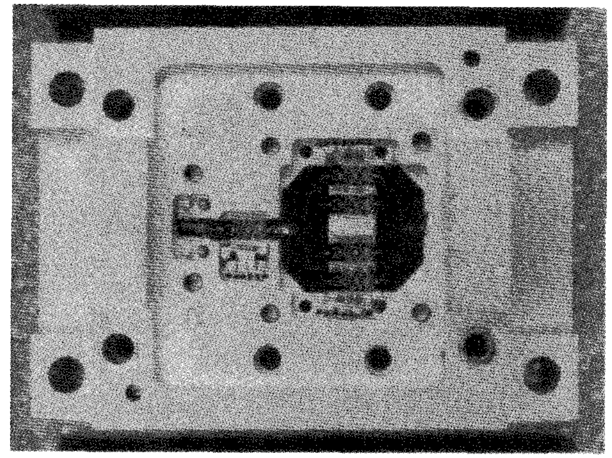

Figure 9. Photograph of power amplifier module.

Power Amplifier Development

The power amplifier was designed for maximum power output while providing narrow bandwidth. The block diagram of the completed amplifier is shown in Figure 8. The amplifier module is a three stage MMIC design consisting of two cascaded amplifiers that are used to drive the four parallel MMICoutput amplifier chips. The first stage is a low power , high gain pre-driver stage that is used to drive the high power driver stage, which drives four identical MMIC amplifiers using the 4-way power divider. The output power is combined using another 4-way power combiner such that the phase at the combining port is equal. For MMIC device selection, the wafer was probed and mapped for the small signal parameters. The selected chips had closely matched phase and gain. A photograph of the amplifier module is shown in Figure 9. DC bias is provided by a voltage divider network that is located on the back side of the amplifier housing.

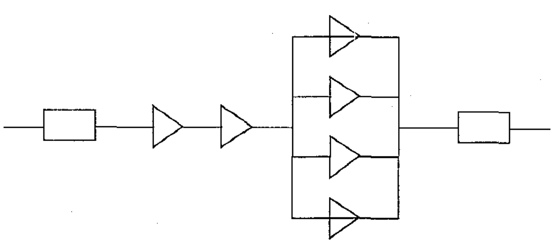

Figure 8. Block diagram of power amplifier module.

The amplifier module demonstrated 100mW of output power with 32 dB gain at ambient temperature, and when cooled to 7°C the measured output power was 140 mW. A plot of the amplifier's output power at ambient is shown in Figure 10. The amplifier housing is a two piece module fabricated from thermcom.,where the higher thermal conductivity of this material allows for more efficient heat transfer. Since this was a prototype amplifier the fused silica substrates, and GaAs MMIC chips and bias components were attached directly to the floor of the housing utilizing conductive epoxy. Using a eutectic solder instead of conductive epoxy to attach the MMIC chips, the efficiency to dissipate heat increases due to the larger thermal conductivity of the solder relative to the epoxy and the output power of the amplifier will increase. Lowloss antipodal finline waveguide-to-microstrip transitions , fabricated on fused silica substrate are located at the amplifier input and output. Typically these transitions have demonstrated ≤0.75 dB insertion loss from 92 GHz to 96 GHz.

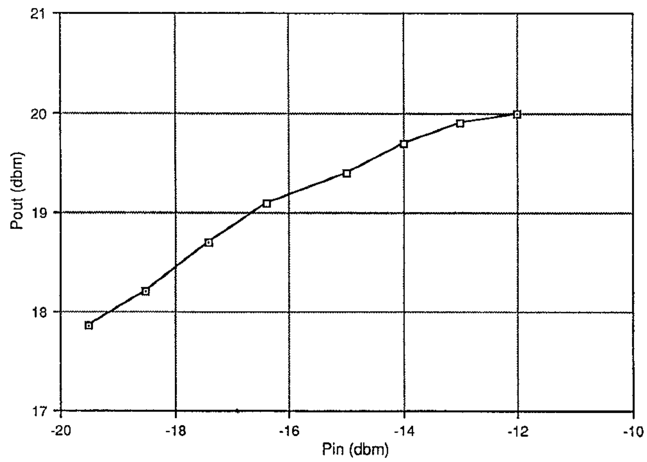

Figure 10. Plot of amplifier output power.

CONCLUSIONS

Excellent RF results have been demonstrated in a small compact SSPA package at W-band The design techniques are flexible and lend themselves to rapid prototyping and design optimization, where this approach can provide increased output power while preserving gain and efficiency.

ACKNOWLEDGMENTS

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